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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,751	02/09/2001	Toshio Yamada	60188-028	5852

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Michael E. Fogarty
McDermott, Will & Emery
600 13th Street, N.W.
Suite 1200
Washington, DC 20005-3096

EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,751	YAMADA, TOSHIO	
	Examiner	Art Unit	
	Lilian Vo	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6, 8 - 11 and 21 - 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6, 8 - 11 and 21 - 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 6, 8 –11 and 21 – 24 are pending. Claims 1 – 5, 7 and 12 – 20 have been cancelled.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 6, 8 –11 and 21 – 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation of transferring the processing specification information and writing resultant processed data through the internal data bus *in a batch*, page 2, lines 7 – 8 and 11 – 12, respectively. Accordingly, there is only one specification information in the first area for transferring (line 2) and probably only one resultant data to be written. Transferring or writing in a batching means mass processing or process in a group. By analyzing the claim languages, it is unclear how single specification information or writing resultant is considered for batch processing as claimed by applicants.

Appropriate clarification is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 , 8, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 5,968,160, hereinafter Saito) in view of Watanabe et al. (US 5,535,410, hereinafter Watanabe).

8. Regarding **claim 6**, Saito teaches the invention as claimed including a data processing method comprising the steps of:

writing a processing specification information in a first area corresponding to a first word line within a semiconductor (col. 6, lines 7 – 9: it's preferred to pack or mount individual constituent elements a single semiconductor integrated circuit substrate. Col. 40, lines 25 – 27) comprising at least one memory array and a data processor coupled to said at least one memory array through at least one internal data bus (fig. 2, B1, col. 7, lines 58 – 63: cache memory is adapted to serve as temporary storage for instruction and the data read out from the main memory. Col. 10, lines 4 – 13: instruction and data is transferring between main memory and the cache. Col. 10, lines 19 – 23, 35 – 40: because instruction cache is a type of memory, it inherently includes at least a word line because word lines, among other components like bit lines, or digit lines, are used for

selecting an addressed memory cell for reading data from or writing data to a memory cell);

writing data to be processed in a second area corresponding to a second word line, which is different from the first word line (fig. 2, B2, col. 10, lines 4 – 6, 28 – 35: because data cache is a type of memory, it inherently includes at least a word line because word lines, among other components like bit lines, or digit lines, are used for selecting an addressed memory cell for reading data from or writing data to a memory cell);

transferring said processing specification information through said at least one internal data bus in a batch to said data processor (fig. 2, b1, A2, col. 10, lines 7 – 13, col. 11, lines 31 – 55: each of the processor elements A2 and A3 executes two instruction in parallel independent of each other);

transferring said data through said at least one internal data bus in a batch to said data processor (fig. 2, b4, A3, col. 9, line 64 – col. 10, lines 49: data cache constituted by a multi-port cache which assumed to have n address input ports and n input/output ports and by employing the multi-port cache as the data cache, reading and writing of data can be performed by n processor elements independently and separately from one another);

processing said data by said data processor using said processing specification information and writing resultant processed data through said at least one internal data bus in a batch in a third area (fig. 2, 3-B, col. 11, lines 30 – 55: each of the processor elements A2 and A3 executes two instructions in parallel independent of each other and storing the results of the arithmetic operations in the register file. Figs 3A and 3B); and

obtaining said resultant processed data by reading said third area after writing said resultant processed data (col. 11, line 31 – col. 12, line 48).

Saito discloses the register file as the third area and did not clearly show this storage is corresponding to a word line. Nevertheless, Watanabe discloses a parallel processor semiconductor chip that process data and store the results or the processed data in the memory with the appropriate word lines (col. 1, lines 31 – 41, fig 2 and col. 5, lines 50 – col. 6, line 37: storing the image data of a single screen in two dimensional memory array FMAR and appropriate word lines of the two dimensional memory array FMAR are selected consecutively to transfer data to the serial access memory SAMout for outputting image data). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made to incorporate Watanabe's teaching with Saito to implement a system with storing the resultant in memory array instead of the register to efficiently utilize the memory cells available from the memory array.

6. Regarding **claim 8**, Saito did not clearly disclose that the second and third area is the same area in which the second area is being overwritten with the resultant processed data. Nevertheless, Watanabe discloses that the second and the third area are the same area and the resultant processed data is being overwritten in the second area (col. 6, lines 7 – 48: if a new screen is displayed or a displayed object is changed, part or all of the contents in the two-dimensional array FMAR must be updated in which pixel data destined to be serially access memory SAMin are written directly to the memory array FMAR). It would have been obvious for one of ordinary skill in the art, at the time the invention was made to incorporate Watanabe's teaching to Saito's system to include the

modification/new data to update the processed resultant so that proper information can be produced/displayed.

7. Regarding **claim 23**, Saito failed to teach that the data processor comprises reconfigurable logic. Nevertheless, Watanabe discloses a parallel processor for performing parallel processing by switching between SIMD and MIMD operations depending on the type of problems to be solved (abstract). It would have been obvious for one of ordinary skill in the art, at the time the invention was made to incorporate this feature to Saito's system so that the system can be dynamically reconfigured to operate in a proper mode for efficiently in keeping with the degree of parallelism of the problem to be solved (Watanabe: abstract and col. 2, lines 3 – 11).

8. Regarding **claim 24**, Saito discloses the data processor comprises a first data processor portion, a second data processor portion and a register coupled between said first and second data processor portions (fig. 3A: A2 – first data processor portion, A3 – second data processor portion, D1 – D4 are registers coupled between A2 and A3. Col. 8, lines 7 – 36: register sharing by these processor elements).

9. Claims 9, 10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 5,968,160, hereinafter Saito) in view of Watanabe et al. (US 5,535,410, hereinafter Watanabe) as applied to claim 6 above, and further in view of Satou et al. (US 5,717,946, hereinafter Satou).

17. Regarding **claim 9**, Saito and Watanabe did not disclose the additional limitation as claimed. Nevertheless, Satou discloses a data processing system wherein said controller reads time information required for said processing to be executed (col. 42, lines 39 – 61, col. 47, lines 4 – 63 and col. 49, lines 9 – 33, and fig. 38, 39 and 44), and reads said resultant processed data written in said third area on the basis of said read time information after time corresponding to said time information elapses (col. 42, lines 23 – 46). It would have been obvious for one of ordinary skill in the art, at the time the invention was made to incorporate the feature in Satou's system to the combination of Saito and Watanabe's invention so that the instructions are processed as high speed by burst transferred between a CPU and a memory (Satou: col. 1, lines 11 – 13).

19. Regarding **claim 10**, Saito and Watanabe failed to teach the feature of storing time information required for each processing to be executed by the semiconductor device. Nevertheless, Satou discloses a data processing system with a table that stores time information required for each processing to be executed (fig. 44). It would have been obvious for one of ordinary skill in the art, at the time the invention was made to incorporate this feature to the combination of Saito and Watanabe's invention to enhance the system performance with the provided timing information.

21. Regarding **claim 22**, Saito discloses the data processing system method of claim 10, wherein said memory network has a bus structure (fig. 2).

10. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 5,968,160, hereinafter Saito) in view of Watanabe et al. (US 5,535,410, hereinafter Watanabe) as applied to claim 6 above, in view of Satou et al. (US 5,717,946, hereinafter Satou), and further in view of Sandberg (US 5,592,625).

23. Regarding **claim 21**, the combination of Saito, Watanabe and Satou failed to teach the memory network has a ring network structure. However, Sandberg teaches the memory network with a ring network structure (col. 3, line 54 – col. 4, line 7). It would have been obvious for one of ordinary skill in the art, at the time the invention was made to incorporate a ring network structure to the combined system of Saito, Watanabe and Satou because it will span larger distance in their network.

11. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 5,968,160, hereinafter Saito) in view of Watanabe et al. (US 5,535,410, hereinafter Watanabe) as applied to claims 6 above, and further in view of Van Doren et al. (US 5,761,731, hereinafter Van Doren).

12. Regarding **claim 11**, although Saito discloses the data processing method of claim 6, except the additional limitation as claimed. Nevertheless, Van Doren discloses a data processing system, in which immediately before executing said processing by said semiconductor device having the data processing function, information describing said processing to be executed is dynamically rewritten for executing said processing (col. 9, lines 45 – 58 and fig. 4). It would have been obvious for one of ordinary skill in the art,

at the time the invention was made to incorporate these features of Van Doren's invention to Saito's system to guarantee data coherency in a system where multiple nodes require atomic transactions (col. 3, lines 21 – 23).

Response to Arguments

13. Applicant's arguments filed on 4/23/04 with respect to claim 6 have been considered but are moot in view of the new ground(s) of rejection.

14. In response to applicant' remarks regarding information on different word lines processing and the semiconductor device (page 8, 1st paragraph), this issues have been addressed in claim 6 rejection above, in which cache memory inherently includes a word line because word lines, among other components like bit lines, or digit lines, are used for selecting an addressed memory cell for reading data from or writing data to a memory cell. As for the limitation semiconductor device, Saito col. 6, lines 7 – 9 discloses that the invention is preferred to pack or mount individual constituent elements a single semiconductor integrated circuit substrate. It is submitted that Saito discloses the limitations as claimed.

15. Regarding applicant's remark (page 9, 2nd paragraph) where applicant points to col. 11, lines 1 – 15 and col. 11, line 56 – col. 12, line 4 to illustrate that Saito cannot process the information in a batch as recited by claim 6, the examiner disagrees. First, col. 11, lines 1 – 15 was never cited in the office action or used in the rejection of claim

6. Beside, this section does not disclose that Saito's system cannot process the information in a batch.

Second, col. 11, line 56 – col. 12, line 4 refers to the case where the register competition or conflict occurs between first and second instructions, in which this is not always the case. Further, col. 12, lines 5 - 19 discloses that the parallel operation control facility has a role or function for clearing or solving such register conflict as mentioned above.

16. Regarding applicant' argument that no writing operation can take in the instruction cache from the processor elements in Saito's system... and that the overhead for rewriting the processing specification is caused in the data processor (page 9, 3rd paragraph), this limitation is nowhere found in claim 6. Claim 6 merely claims the step of writing the specification in the first area within a semiconductor device that comprising a processor coupling to the memory array, in which Saito col. 7, lines 58 – 63 discloses that instruction are loading/transferring from the memory main to the cache (see also col. 10, lines 4 – 13 and fig.1, A4 and A5).

Furthermore, Saito also teaches the step of processing said data by said data processor using said processing specification information and writing resultant processed data as shown in col. 11, lines 30 – 55 in which each of the processor elements A2 and A3 executes two instructions in parallel independent of each other and storing the results of the arithmetic operations in the register file (see also figs 3A and 3B). Therefore, Saito disclosure clearly read on the claim limitations.

17. Regarding applicant's remarks in which claim 24 is patentably distinct over Saito because applicant's invention is about the configuring the data transfer the memory arrays or buses with hyper-wide bit registers that aligned at the center (page 11, 1st paragraph), the examiner disagrees. First, the argument with such limitation is nowhere found in the claim. Second, claim 24 merely claims a data processing with a register coupling between the two data processor portions. Saito's disclosure clearly read on the claim limitation in which he shows the registers or the sharing registers coupling between the two processor elements in fig. 3A and col. 8, lines 7 – 36.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Ooishi (US Pat. Application Publication 2002/0075746) disclosed a data processing with a semiconductor device that refreshes and rewrite instruction processing in the memory array.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 703-305-7864. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 703-305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2127

lv
August 19, 2004

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100